



中显液晶  
技术资料



## 型号ZX320240C

2009年3月15日

北京市海淀区中关村大街32号和盛大厦811室  
电话：(86)-010-52926620 传真：(86)-010-52926621  
企业网站：<http://www.zxlcd.com>

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## RECORDS OF REVISION

DATE	REVISED NO.	REVISED DESCRIPTIONS	PREPARED	CHECKED	APPROVED
March 22, 2008	1.00	FIRST ISSUE	YNN		

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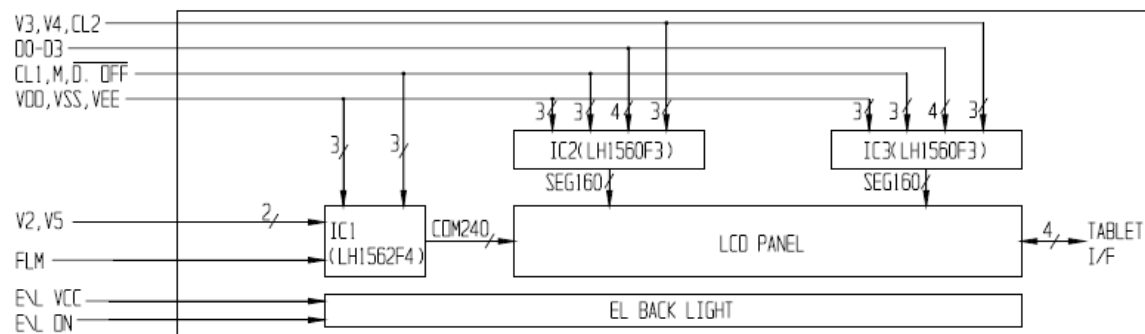
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## 1 FEATURES :

ITEM	STANDARD VALUE	UNIT
Display Type	320 *240 dots	-
LCD Type	<input type="checkbox"/> STN, BLUE, Transflective, Negative, Extend TEMP <input type="checkbox"/> STN, YELLOW-GREEN, Transflective, Position, Extend TEMP <input checked="" type="checkbox"/> FSTN, Transflective, Position, Extend TEMP	-
LCD Duty	1/240	-
LCD Bias	1/13	-
Viewing Direction	6:00	-
Backlight Type	CCFL(White)	-
Module Dimension	70.5(W) X89.0(H) X7.3(MAX)(T)	mm
Viewing Area	61.1(W)X80.55(H)	mm
Dot Size	0.225(W) X 0.225(H)	mm
Dot Pitch	0.24(W) X 0.24(H)	mm

## 2.BLOCK DIAGRAM



## 3.ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Supply voltage for logic	VDD	-0.3	7.0	V
Supply voltage for LCD	VDD-V0	-0.3	+45.0	V
Input voltage	VI	-0.3	VDD+0.3	V
Operating temperature	TOP	-20	70	°C
Storage temperature	TST	-30	80	°C

## 4.ELECTRICAL CHARACTERISTICS

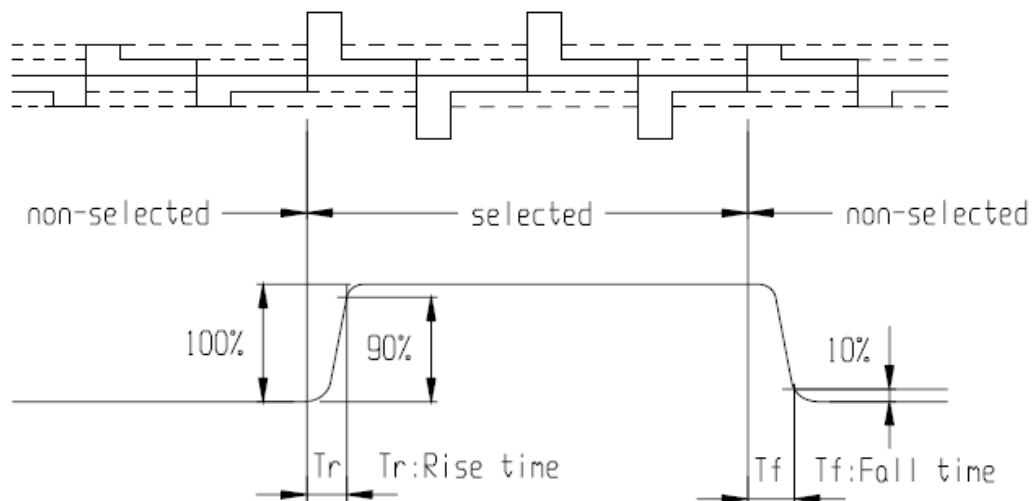
(VDD=+3V±10% or VDD=+5V±10%, VSS=0V, Ta=25°C)

Model No.	Panel	Duty ratio	Drive function	Common /Segment	Data input	Mzimum display voltage(V)	Maximum clock frequency(MHz)	Supply Voltage(V)
LH1560F3	Large	to 1/480	Segment/ Common	240	4/8-bit paralld(a t segment drive)	+42	Segment mode 8(at 2.5V) 14(at 5V) Common mode 4	2.5 to 5.5

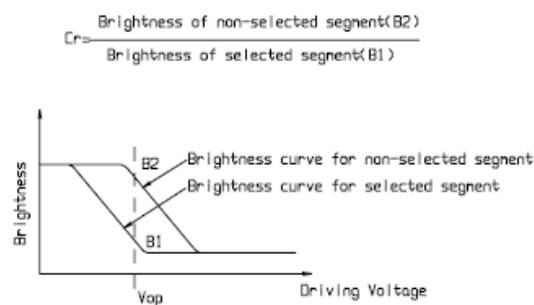
## 5.ELECTRO-OPTICAL CHARACTERISTICS(Vop=20.8V,Ta=25°C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks	Note
Response Time	Tr	---	---	384	---	ms	---	1
	Tf	---	---	220	---	ms	---	1
Contrast Ratio	Cr	---	---	4.6	---	---	---	2
Viewing Angle Range	$\theta$	$Cr \geq 2$	20	---	---	deg	$\phi = 90^\circ$	3
			34	---	---	deg	$\phi = 270^\circ$	3
			56	---	---	deg	$\phi = 0^\circ$	3
			33	---	---	deg	$\phi = 180^\circ$	3

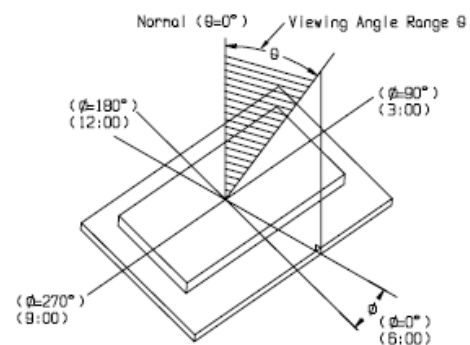
Note 1. Definition of response time



Note 2. Definition of Contrast Ratio 'Cr'



Note 3. Definition of Viewing Angle Range ' $\theta$ '



## 6.TIMING CHARACTERISTICS

### 6.1 DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage for logic	VDD	---	2.7	5.0	5.5	V
Supply current for logic	IDD	---	---	400	500	uA
Operating voltage for LCD	VDD - VO	0°C	20.4	21.5	22.6	V
		25°C	19.6	20.7	21.8	V
		50°C	18.8	19.9	21.0	V
Input voltage 'H' level	VIH	---	0.7VDD	---	VDD	V
Input voltage 'L' level	VIL	---	0	---	0.3VDD	V
EL Enable voltage (ON)	EON	---	---	100	150	V
EL frequency	LF	---	---	400	1000	Hz

(Segment Mode) (VSS = V5 = 0 V, VDD = +2.5 to +5.5 V, V0 = +15.0 to +42.0 V, TOPR = -20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	VIL		DI7-DI0, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, DISPOFF			0.2VDD	V	
Input "High" voltage	VIH			0.8VDD			V	
Output "Low" voltage	VOL	IOL = +0.4 mA	EIO1, EIO2			+0.4	V	
Output "High" voltage	VOH	IOH = -0.4 mA		VDD - 0.4			V	
Input leakage current	ILIL	VI = VSS	DI7-DI0, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, DISPOFF			-10.0	μA	
	ILIH	VI = VDD				+10.0	μA	
Output resistance	RON	$\frac{\Delta V_{ON}}{I} = 0.5 \text{ V}$	Y1-Y240		1.0	1.5	kΩ	
		V0 = 40 V			1.5	2.0		
		V0 = 30 V			2.0	2.5		
Standby current	ISTB		VSS			75.0	μA	1
Supply current (1) (Non-selection)	IDD1		VDD			2.0	mA	2
Supply current (2) (Selection)	IDD2		VDD			12.0	mA	3
Supply current (3)	I0		VOL, VOR			1.5	mA	4

#### NOTES :

- VDD = +5.0 V, V0 = +42.0 V, VI = VSS.
- VDD = +5.0 V, V0 = +42.0 V, fXCK = 20 MHz, no-load, EI = VDD.  
The input data is turned over by data taking clock (4-bit parallel input mode).
- VDD = +5.0 V, V0 = +42.0 V, fXCK = 20 MHz, no-load, EI = VSS.  
The input data is turned over by data taking clock (4-bit parallel input mode).
- VDD = +5.0 V, V0 = +42.0 V, fXCK = 20 MHz, fLP = 41.6 kHz, fFR = 80 Hz, no-load.  
The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) ( $V_{SS} = V_5 = 0\text{ V}$ ,  $V_{DD} = +2.5\text{ to }+5.5\text{ V}$ ,  $V_0 = +15.0\text{ to }+42.0\text{ V}$ ,  $T_{OPR} = -20\text{ to }+85\text{ }^{\circ}\text{C}$ )

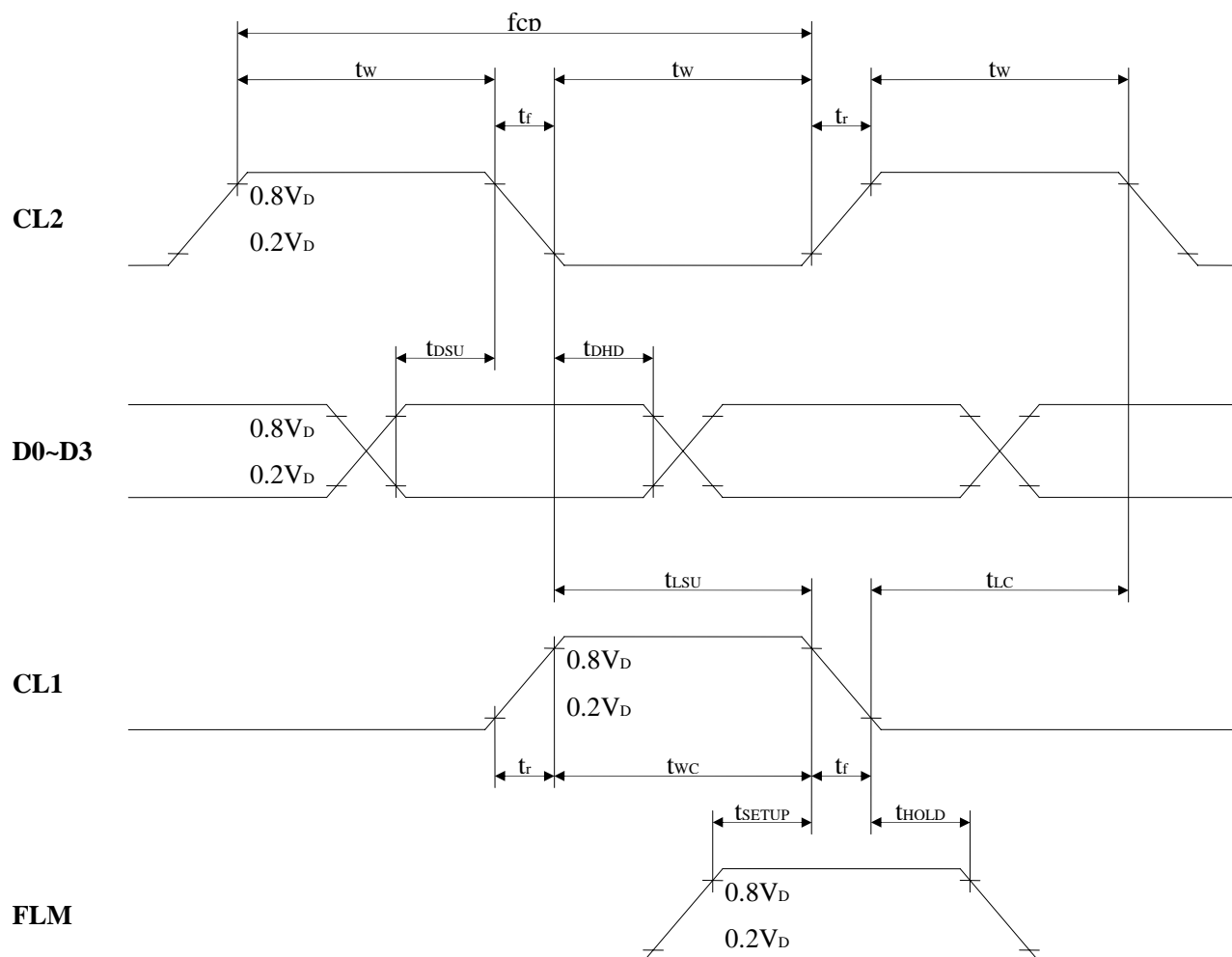
PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	$V_{IL}$		DI7-DI0, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, $\overline{\text{DISPOFF}}$			$0.2V_{DD}$	V	
Input "High" voltage	$V_{IH}$			$0.8V_{DD}$			V	
Output "Low" voltage	$V_{OL}$	$I_{OL} = +0.4\text{ mA}$	EIO1, EIO2			+0.4	V	
Output "High" voltage	$V_{OH}$	$I_{OH} = -0.4\text{ mA}$		$V_{DD} - 0.4$			V	
Input leakage current	$I_{LIL}$	$V_i = V_{SS}$	DI7-DI0, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, $\overline{\text{DISPOFF}}$			-10.0	$\mu\text{A}$	
	$I_{LIH}$	$V_i = V_{DD}$	DI6-DI0, LP, L/R, FR, MD, S/C, $\overline{\text{DISPOFF}}$			+10.0	$\mu\text{A}$	
Input pull-down current	$I_{PD}$	$V_i = V_{DD}$	DI7, XCK, EIO1, EIO2			100.0	$\mu\text{A}$	
Output resistance	$R_{ON}$	$ \Delta V_{ON}  = 0.5\text{ V}$	Y1-Y240		1.0	1.5	k $\Omega$	
					1.5	2.0		
					2.0	2.5		
Standby current	$I_{STB}$		$V_{SS}$			75.0	$\mu\text{A}$	1
Supply current (1)	$I_{DD}$		$V_{DD}$			120.0	$\mu\text{A}$	2
Supply current (2)	$I_0$		$V_{OL}$ , $V_{OR}$			240.0	$\mu\text{A}$	2

#### NOTES :

1.  $V_{DD} = +5.0\text{ V}$ ,  $V_0 = +42.0\text{ V}$ ,  $V_i = V_{SS}$
2.  $V_{DD} = +5.0\text{ V}$ ,  $V_0 = +42.0\text{ V}$ ,  $f_{LP} = 41.6\text{ kHz}$ ,  $f_{FR} = 80\text{ Hz}$ , 1/480 duty operation, no-load.

## 6.2 AC Characteristics

Item	Symbol	Min	Typ	Max	Unit
CL1 pulse width 掣”	tw	23	---	---	ns
Clock cycle time	f <sub>CP</sub>	71	---	---	ns
CL2 pulse width	twc	23	---	---	ns
Clock set up time	t <sub>LSU</sub>	25	---	---	ns
Clock hole time	t <sub>LC</sub>	25	---	---	ns
Clock rise/fall time	t <sub>r</sub> , t <sub>f</sub>	---	---	50	ns
Data set up time	t <sub>DSU</sub>	10	---	---	ns
Data hold time	t <sub>DHD</sub>	20	---	---	ns
' M ' set up time	t <sub>SETUP</sub>	25	---	---	ns
' M ' hold time	t <sub>HOLD</sub>	25	---	---	ns



(Segment Mode 1) ( $V_{SS} = V_5 = 0\text{ V}$ ,  $V_{DD} = +5.0 \pm 0.5\text{ V}$ ,  $V_0 = +15.0\text{ to }+42.0\text{ V}$ ,  $T_{OPR} = -20\text{ to }+85\text{ }^\circ\text{C}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	$t_{wCK}$	$t_r, t_f \leq 10\text{ ns}$	50			ns	1
Shift clock "H" pulse width	$t_{wCKH}$		15			ns	
Shift clock "L" pulse width	$t_{wCKL}$		15			ns	
Data setup time	$t_{DS}$		10			ns	
Data hold time	$t_{DH}$		12			ns	
Latch pulse "H" pulse width	$t_{WLPH}$		15			ns	
Shift clock rise to latch pulse rise time	$t_{LD}$		0			ns	
Shift clock fall to latch pulse fall time	$t_{SL}$		30			ns	
Latch pulse rise to shift clock rise time	$t_{LS}$		25			ns	
Latch pulse fall to shift clock fall time	$t_{LH}$		25			ns	
Enable setup time	$t_s$		10			ns	
Input signal rise time	$t_r$				50	ns	2
Input signal fall time	$t_f$				50	ns	2
DISPOFF removal time	$t_{SD}$		100			ns	
DISPOFF "L" pulse width	$t_{WDL}$		1.2			$\mu\text{s}$	
Output delay time (1)	$t_D$	$C_L = 15\text{ pF}$			30	ns	
Output delay time (2)	$t_{PD1}, t_{PD2}$	$C_L = 15\text{ pF}$			1.2	$\mu\text{s}$	
Output delay time (3)	$t_{PD3}$	$C_L = 15\text{ pF}$			1.2	$\mu\text{s}$	

#### NOTES :

1. Takes the cascade connection into consideration.
2.  $(t_{wCK} - t_{wCKH} - t_{wCKL})/2$  is maximum in the case of high speed operation.



(Segment Mode 2) ( $V_{SS} = V_5 = 0\text{ V}$ ,  $V_{DD} = +3.0\text{ to }+4.5\text{ V}$ ,  $V_0 = +15.0\text{ to }+42.0\text{ V}$ ,  $T_{OPR} = -20\text{ to }+85\text{ }^{\circ}\text{C}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	twck	$t_R, t_F \leq 10\text{ ns}$	66			ns	1
Shift clock "H" pulse width	twckH		23			ns	
Shift clock "L" pulse width	twckL		23			ns	
Data setup time	tds		15			ns	
Data hold time	tdh		23			ns	
Latch pulse "H" pulse width	twLPH		30			ns	
Shift clock rise to latch pulse rise time	tLD		0			ns	
Shift clock fall to latch pulse fall time	tSL		50			ns	
Latch pulse rise to shift clock rise time	tLS		30			ns	
Latch pulse fall to shift clock fall time	tLH		30			ns	
Enable setup time	ts		15			ns	
Input signal rise time	tR				50	ns	2
Input signal fall time	tF				50	ns	2
DISPOFF removal time	tsd		100			ns	
DISPOFF "L" pulse width	twDL		1.2			$\mu\text{s}$	
Output delay time (1)	td	$C_L = 15\text{ pF}$			41	ns	
Output delay time (2)	tpD1, tpD2	$C_L = 15\text{ pF}$			1.2	$\mu\text{s}$	
Output delay time (3)	tpD3	$C_L = 15\text{ pF}$			1.2	$\mu\text{s}$	

**NOTES :**

1. Takes the cascade connection into consideration.
2.  $(twck - twckH - twckL)/2$  is maximum in the case of high speed operation.

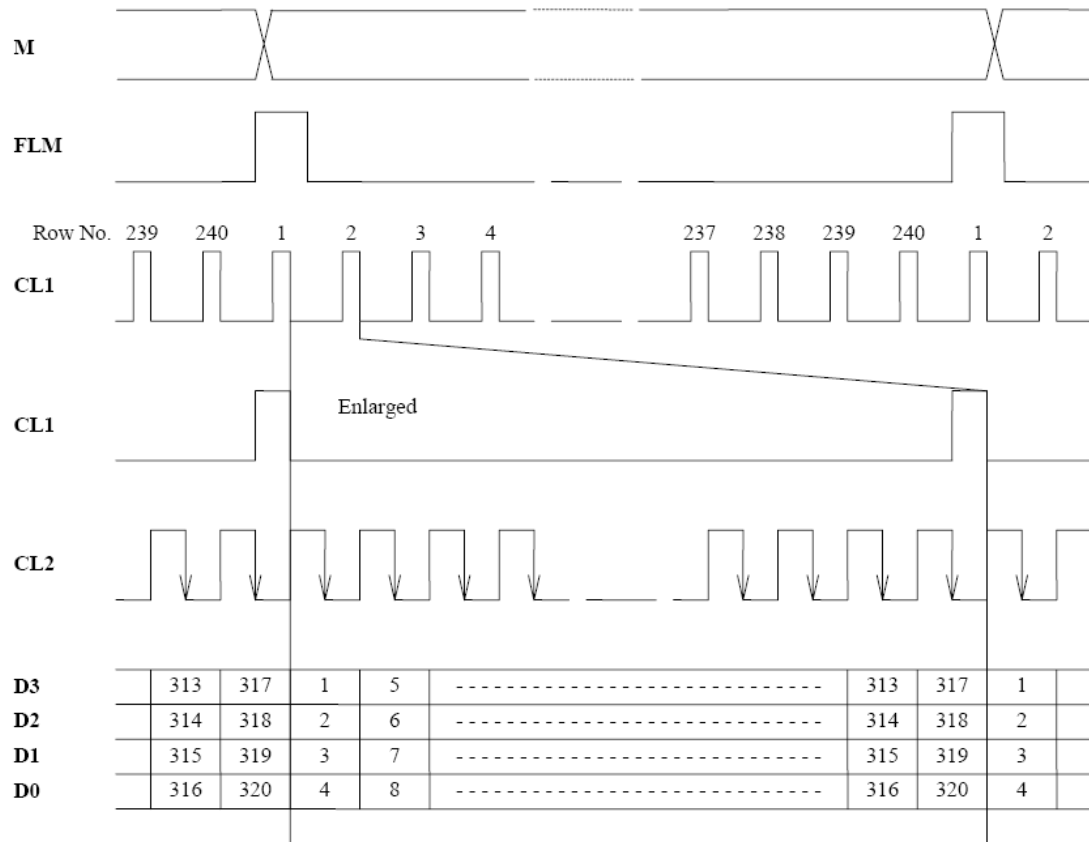
(Segment Mode 3) ( $V_{SS} = V_5 = 0\text{ V}$ ,  $V_{DD} = +2.5\text{ to }+3.0\text{ V}$ ,  $V_0 = +15.0\text{ to }+42.0\text{ V}$ ,  $T_{OPR} = -20\text{ to }+85\text{ }^{\circ}\text{C}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	twck	$t_R, t_F \leq 10\text{ ns}$	82			ns	1
Shift clock "H" pulse width	twckH		28			ns	
Shift clock "L" pulse width	twckL		28			ns	
Data setup time	tds		20			ns	
Data hold time	tdh		23			ns	
Latch pulse "H" pulse width	twLPH		30			ns	
Shift clock rise to latch pulse rise time	tLD		0			ns	
Shift clock fall to latch pulse fall time	tSL		65			ns	
Latch pulse rise to shift clock rise time	tLS		30			ns	
Latch pulse fall to shift clock fall time	tLH		30			ns	
Enable setup time	ts		15			ns	
Input signal rise time	tR				50	ns	2
Input signal fall time	tF				50	ns	2
DISPOFF removal time	tsd		100			ns	
DISPOFF "L" pulse width	twDL		1.2			$\mu\text{s}$	
Output delay time (1)	td	$C_L = 15\text{ pF}$			57	ns	
Output delay time (2)	tpD1, tpD2	$C_L = 15\text{ pF}$			1.2	$\mu\text{s}$	
Output delay time (3)	tpD3	$C_L = 15\text{ pF}$			1.2	$\mu\text{s}$	

**NOTES :**

1. Takes the cascade connection into consideration.
2.  $(twck - twckH - twckL)/2$  is maximum in the case of high speed operation.

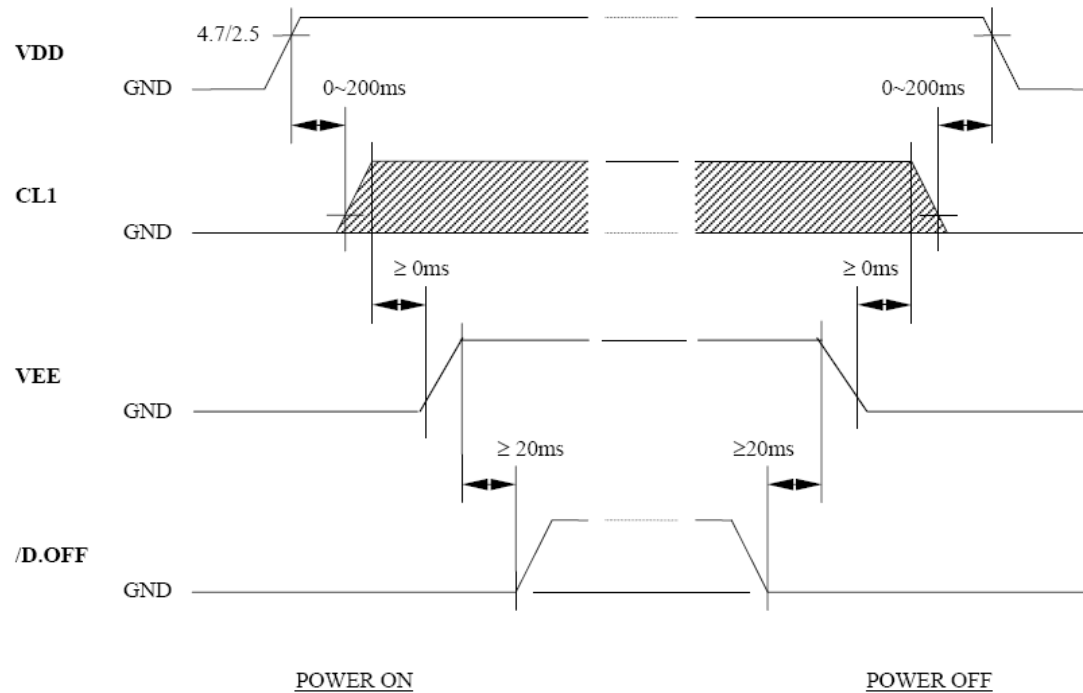
### 6.3 Timing Chart of Input Signal



### 6.4 Display Data Pattern

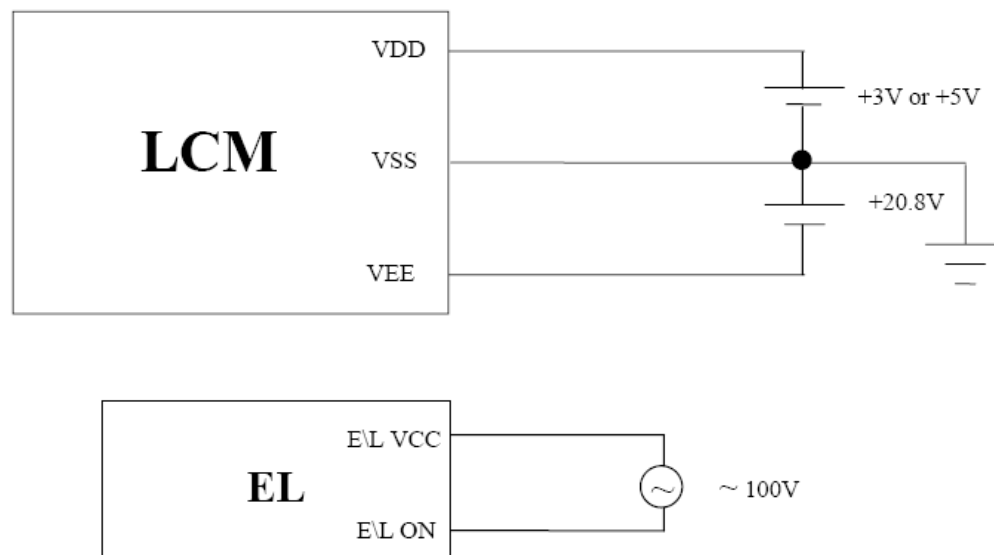
	S1	S2	S3	S4	S5	• • • • •	S316	S317	S318	S319	S320	SEG																																		
C1	D3	D2	D1	D0	D3	• • • • •	D0	D3	D2	D1	D0																																			
C2	D3	D2	D1	D0	D3	• • • • •	D0	D3	D2	D1	D0																																			
• • • • • • •	<table><tr><td>Input data</td><td colspan="6">Dots on display</td></tr><tr><td>D0</td><td>Dot 4</td><td>Dot 8</td><td>• • •</td><td>Dot 316</td><td colspan="2">Dot 320</td></tr><tr><td>D1</td><td>Dot 3</td><td>Dot 7</td><td>• • •</td><td>Dot 315</td><td colspan="2">Dot 319</td></tr><tr><td>D2</td><td>Dot 2</td><td>Dot 6</td><td>• • •</td><td>Dot 314</td><td colspan="2">Dot 318</td></tr><tr><td>D3</td><td>Dot 1</td><td>Dot 5</td><td>• • •</td><td>Dot 313</td><td colspan="2">Dot 317</td></tr></table>												Input data	Dots on display						D0	Dot 4	Dot 8	• • •	Dot 316	Dot 320		D1	Dot 3	Dot 7	• • •	Dot 315	Dot 319		D2	Dot 2	Dot 6	• • •	Dot 314	Dot 318		D3	Dot 1	Dot 5	• • •	Dot 313	Dot 317
Input data	Dots on display																																													
D0	Dot 4	Dot 8	• • •	Dot 316	Dot 320																																									
D1	Dot 3	Dot 7	• • •	Dot 315	Dot 319																																									
D2	Dot 2	Dot 6	• • •	Dot 314	Dot 318																																									
D3	Dot 1	Dot 5	• • •	Dot 313	Dot 317																																									
C239	D3	D2	D1	D0	D3	• • • • •	D0	D3	D2	D1	D0																																			
C240	D3	D2	D1	D0	D3	• • • • •	D0	D3	D2	D1	D0																																			
COM																																														

## 6.5 Timing of Power Supply



Note : The missing pixels may occur when the LCM is driven except above power supply timing sequence.

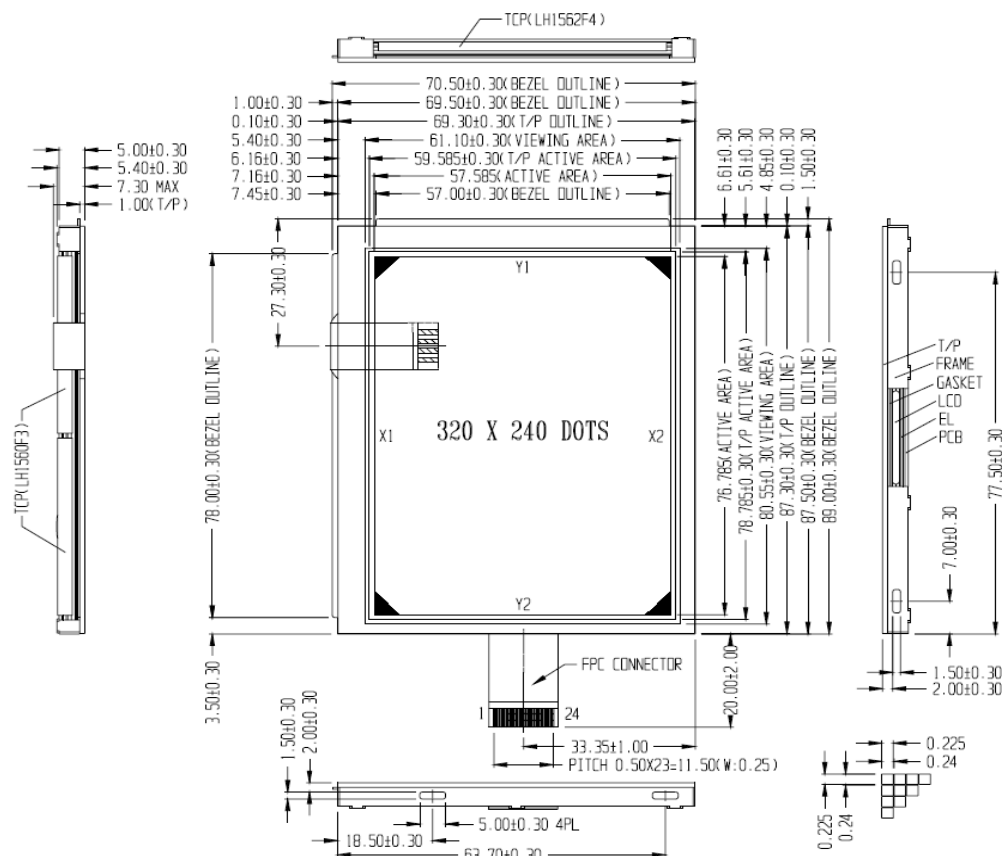
## 6.6 Example of Power Connection



## 7. PIN ASSIGNMENT

Pin No.	Symbol	Level	Description
1	V5	---	Power supply pin for LCD driver voltage bias (VSS<V5<V4<V3<V2<VEE)
2	V2	---	Power supply pin for LCD driver voltage bias (VSS<V5<V4<V3<V2<VEE)
3	VEE	+20.8V	Power supply pin for LCD driver voltage
4	VDD	+5V or +3V	Logic system power supply pin
5	FLM	H/L	Frame signal pin
6	VSS	0V	Ground
7	CL1	H/L	Latch pulse input pin for display data
8	VSS	0V	Ground
9	M	H/L	AC signal input for LCD driving waveform
10	/D.OFF	L	Control input pin for output deselect level
11	CL2	H/L	Clock input pin for taking display data
12	V4	---	Power supply pin for lcd driver voltage bias (VSS<V5<V4<V3<V2<VEE)
13	V3	---	Power supply pin for lcd driver voltage bias (VSS<V5<V4<V3<V2<VEE)
14	D3	H/L	Data bit 4
15	D2	H/L	Data bit 3
16	D1	H/L	Data bit 2
17	D0	H/L	Data bit 1
18	NC	---	No connection
19	T/P(X2)	---	No connection
20	T/P(Y1)	---	No connection
21	T/P(X1)	---	No connection
22	T/P(Y2)	---	No connection
23	E/L VCC	AC	EL light AC supply pin
24	E/L ON	AC	EL light AC supply pin

## 8. OUTLINE DIMENSIONS



## 9. RELIABILITY

### Content of Reliability Test

Environmental Test				
No.	Test Item	Content of Test	Test Condition	Applicable Standard
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	80 °C 200 hrs	
2	Low temperature storage	Endurance test applying the low storage temperature for a long time.	-30 °C 200 hrs	
3	High temperature operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70 °C 200 hrs	
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time.	-20 °C 200 hrs	
5	High temperature Humidity storage	Endurance test applying the high temperature and high humidity storage for a long time.	50 °C , 90% RH 96 hrs	MIL-202E-103B JIS-C5023
6	High temperature Humidity operation	Endurance test applying the electric stress (Voltage & Current) and temperature humidity stress to the element for a long time.	50 °C , 90% RH 96 hrs	MIL-202E-103B JIS-C5023
7	Temperature cycle	Endurance test applying the low and high temperature cycle. <div style="text-align: center;">           -20°C      25°C      70°C  <math>\xleftarrow{30\text{min.}} \rightleftharpoons 5\text{min.} \rightleftharpoons \xrightarrow{30\text{min.}}</math>            1 cycle         </div>	-20°C – 70°C 10 cycles	
Mechanical Test				
8	Vibration test	Endurance test applying the vibration during transportation and using.	10-22Hz → 1.5mmp-p 22-500Hz → 1.5G Total 0.5hrs	MIL-202E-201A JIS-C5025 JIS-C7022-A-10

9	Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G half sign wave 1l msdc 3 times of each direction	MIL-202E-213B
10	Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115 mbar 40 hrs	MIL-202E-105C
<b>Others</b>				
11	Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V, RS=1.5 k CS=100 pF 1 time	MIL-883B-3015.1

Supply voltage for logic system = 3V. Supply voltage for LCD system = Operating voltage at 25°C.

## 10. QUALITY GUARANTEE

### Acceptable Quality Level

Each lot should satisfy the quality level defined as follows.

- Inspection method : MIL-STD-105E LEVEL II Normal one time sampling
- AQL

Partition	AQL	Definition
A: Major	0.4%	Functional defective as product
B: Minor	1.5%	Satisfy all functions as product but not satisfy cosmetic standard

### Definition of 'LOT'

One lot means the delivery quantity to customer at one time.

### Conditions of Cosmetic Inspection

#### Environmental condition

The inspection should be performed at the 1cm of height from the LCD module under 2 pieces of 40W white fluorescent lamps (Normal temperature 20~25°C and normal humidity 60±15%RH).

#### Inspection method

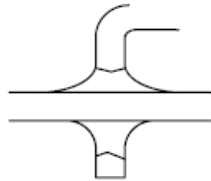
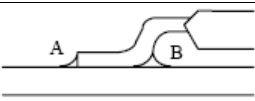
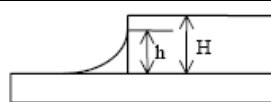
The visual check should be performed vertically at more than 30cm distance from the LCD panel.

### Driving voltage

The VO value which the most optimal contrast can be obtained near the specified VO in the specification. (Within  $\pm 0.5V$  of typical value at 25°C.).

## 11. INSPECTION CRITERIA

### 11.1 Module Cosmetic Criteria

No.	Item	Judgement Criterion	Partition
1	Difference in Spec.	None allowed	Major
2	Pattern peeling	No substrate pattern peeling and floating	Major
3	Soldering defects	No soldering missing No soldering bridge No cold soldering	Major Major Major
4	Resist flaw on substrate	Invisible copper foil ('0.5mm or more) on substrate pattern	Minor
5	Accretion of metallic Foreign matter	No soldering dust No accretion of metallic foreign matters (Not exceed '0.2mm)	Minor Minor
6	Stain	No stain to spoil cosmetic badly	Minor
7	Plate discoloring	No plate fading, rusting and discoloring	Minor
8	Solder amount	a. Soldering side of PCB Solder to form a 'Filet' all around the lead. Solder should not hide the lead form perfectly. (too much) b. Components side ( In case of 'Through Hole PCB' ) 	Minor
	1. Lead parts	Solder to reach the Components side of PCB.	
	2. Flat packages	Either 'Toe' (A) or 'Seal' (B) of the lead to be covered by 'Filet'.  Lead form to be assume over solder. A B	Minor
	3. Chips	$(3/2) H \geq h \geq (1/2) H$ 	Minor

## 11.2 Screen Cosmetic Criteria (Non-Operating)

No.	Defect	Judgement Criterion	Partition										
1	Spots	In accordance with <i>Screen Cosmetic Criteria (Operating) No.1.</i>	Minor										
2	Lines	In accordance with <i>Screen Cosmetic Criteria (Operating) No.2.</i>	Minor										
3	Bubbles in polarizer	<table><tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr><tr><td><math>d \leq 0.3</math></td><td>Disregard</td></tr><tr><td><math>0.3 &lt; d \leq 1.0</math></td><td>3</td></tr><tr><td><math>1.0 &lt; d \leq 1.5</math></td><td>1</td></tr><tr><td><math>1.5 &lt; d</math></td><td>0</td></tr></table>	Size : d mm	Acceptable Qty in active area	$d \leq 0.3$	Disregard	$0.3 < d \leq 1.0$	3	$1.0 < d \leq 1.5$	1	$1.5 < d$	0	Minor
Size : d mm	Acceptable Qty in active area												
$d \leq 0.3$	Disregard												
$0.3 < d \leq 1.0$	3												
$1.0 < d \leq 1.5$	1												
$1.5 < d$	0												
4	Scratch	In accordance with spots and lines operating cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor										
5	Allowable density	Above defects should be separated more than 30mm each other.	Minor										
6	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-lit type should be judged with back-lit on state only.	Minor										
7	Contamination	Not to be noticeable.	Minor										

## 12.3. Screen Cosmetic Criteria (Operating)

No.	Defect	Judgement Criterion	Partition																				
1	Spots	<div>A) Clear Note :</div> <table><tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr><tr><td><math>d \leq 0.1</math></td><td>Disregard</td></tr><tr><td><math>0.1 &lt; d \leq 0.2</math></td><td>3</td></tr><tr><td><math>0.2 &lt; d \leq 0.3</math></td><td>2</td></tr><tr><td><math>0.3 &lt; d</math></td><td>0</td></tr></table> <div>Including pin holes and defective dots which must be within one pixel size.</div> <div>B) Unclear Size :</div> <table><tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr><tr><td><math>d \leq 0.2</math></td><td>Disregard</td></tr><tr><td><math>0.2 &lt; d \leq 0.5</math></td><td>6</td></tr><tr><td><math>0.5 &lt; d \leq 0.7</math></td><td>2</td></tr><tr><td><math>0.7 &lt; d</math></td><td>0</td></tr></table>	Size : d mm	Acceptable Qty in active area	$d \leq 0.1$	Disregard	$0.1 < d \leq 0.2$	3	$0.2 < d \leq 0.3$	2	$0.3 < d$	0	Size : d mm	Acceptable Qty in active area	$d \leq 0.2$	Disregard	$0.2 < d \leq 0.5$	6	$0.5 < d \leq 0.7$	2	$0.7 < d$	0	Minor
Size : d mm	Acceptable Qty in active area																						
$d \leq 0.1$	Disregard																						
$0.1 < d \leq 0.2$	3																						
$0.2 < d \leq 0.3$	2																						
$0.3 < d$	0																						
Size : d mm	Acceptable Qty in active area																						
$d \leq 0.2$	Disregard																						
$0.2 < d \leq 0.5$	6																						
$0.5 < d \leq 0.7$	2																						
$0.7 < d$	0																						



2	Lines	<p>A) Clear</p> <p>Note : ( ) - Acceptable Qty in active area L  - Length (mm) W - Width (mm)  <math>\infty</math> - Disregard</p> <p>B) Unclear</p>	Minor
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‘Clear’ = The shade and size are not changed by VO.

‘Unclear’ = The shade and size are changed by VO.

#### 11.4. Screen Cosmetic Criteria (Operating) (Continued)

No.	Defect	Judgement Criterion	Partition
3	Rubbing line	Not to be noticeable.	
4	Allowable density	Above defects should be separated more than 10mm each other.	Minor
5	Rainbow	Not to be noticeable.	Minor
6	Dot size	To be 95% ~ 105% of the dot size (Typ.) in drawing. Partial defects of each dot (ex. pin-hole) should be treated as ‘Spot’. (see <i>Screen Cosmetic Criteria (Operating) No.1</i> )	Minor
7	Uneven brightness (only back-lit type module)	<p>Uneven brightness must be <math>B_{MAX} / B_{MIN} \leq 2</math></p> <ul style="list-style-type: none"> <li>- <math>B_{MAX}</math> : Max. value by measure in 5 points</li> <li>- <math>B_{MIN}</math> : Min. value by measure in 5 points</li> </ul> <p>Divide active area into 4 vertically and horizontally. Measure 5 points shown in the following figure.</p> <p>○ : Measuring points</p>	Minor

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Note :

- (1) Size :  $d = (\text{long length} + \text{short length}) / 2$
- (2) The limit samples for each item have priority.
- (3) Complexed defects are defined item by item, but if the number of defects are defined in above table, the total number should not exceed 10.
- (4) In case of 'concentration', even the spots or the lines of 'disregarded' size should be not allowed. Following three situations should be treated as 'concentration'.
  - 7 or over defects in circle of '5mm.
  - 10 or over defects in circle of '10mm.
  - 20 or over defects in circle of '20mm.

## 12. PRECAUTIONS FOR USING LCD MODULES

### Handling Precautions

- (1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.
- (2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.
- (3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- (4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- (5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents :
  - Isopropyl alcohol
  - Ethyl alcohol
- (6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.
  - Water
  - Ketone
  - Aromatic solvents
- (7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.
- (8) Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.
- (9) Do not attempt to disassemble or process the LCD module.
- (10) NC terminal should be open. Do not connect anything.
- (11) If the logic circuit power is off, do not apply the input signals.
- (12) To prevent destruction of the elements by static electricity, be careful to maintain

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an optimum work environment.

- Be sure to ground the body when handling the LCD modules.
- Tools required for assembling, such as soldering irons, must be properly grounded.
- To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.
- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

### **Storage Precautions**

When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags (avoid high temperature high humidity and low temperatures below 0 °C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

### **Others**

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature.

If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.

To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity etc., exercise care to avoid holding the following sections when handling the modules.

- Exposed area of the printed circuit board.
- Terminal electrode sections.

## **13. USING LCD MODULES**

### **Liquid Crystal Display Modules**

LCD is composed of glass and polarizer. Pay attention to the following items when handling.

- (1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.
- (2) Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead (glass, tweezers, etc.).
- (3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizers and reflectors made of organic substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropylalcohol.
- (4) When the display surface becomes dusty, wipe gently with absorbent cotton or

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other soft material like chamois soaked in petroleum benzin. Do not scrub hard to avoid damaging the display surface.

(5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.

(6) Avoid contacting oil and fats.

(7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperature they must be warmed up in a container before coming in contact with room temperature air.

(8) Do not put or attach anything on the display area to avoid leaving marks on.

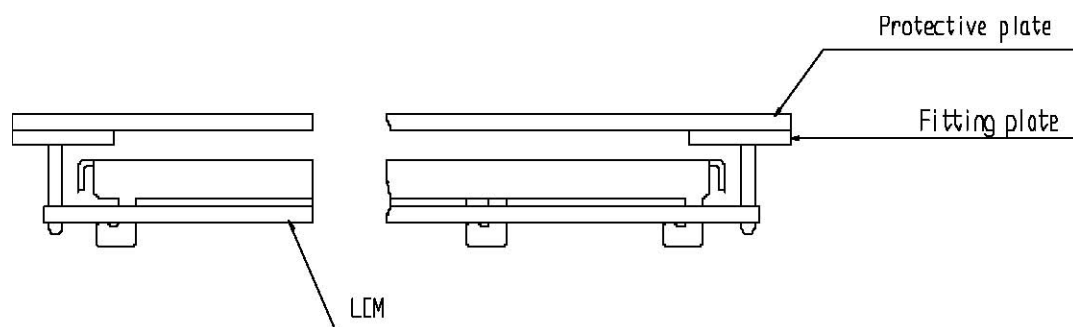
(9) Do not touch the display with bare hands. This will stain the display area and degrade insulation between terminals (some cosmetics are detrimental to the polarizers).

(10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

### Installing LCD Modules

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be 0.1mm.

### Precaution for Handling LCD Modules

Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.

(1) Do not alter, modify or change the shape of the tab on the metal frame.

(2) Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.

(3) Do not damage or modify the pattern writing on the printed circuit board.

(4) Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector.

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(5) Except for soldering the interface, do not make any alterations or modifications with a soldering iron.

(6) Do not drop, bend or twist LCM.

#### **Electro-Static Discharge Control**

Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

(1) Make certain that you are grounded when handling LCM.

(2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.

(3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.

(4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutator of the motor.

(5) As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.

(6) To reduce the generation of static electricity be careful that the air in the work is not too dried. A relative humidity of 50%60% is recommended.

#### **Precaution for soldering to the LCM**

(1) Observe the following when soldering lead wire, connector cable and etc. to the LCM.

- Soldering iron temperature : 280 C 10 C.
- Soldering time : 3-4 sec.
- Solder : eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

(2) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.

(3) When remove the electroluminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PC board could be damaged.

#### **Precautions for Operation**

(1) Viewing angle varies with the change of liquid crystal driving voltage (VO). Adjust VO to show the best contrast.

(2) Driving the LCD in the voltage above the limit shortens its life.

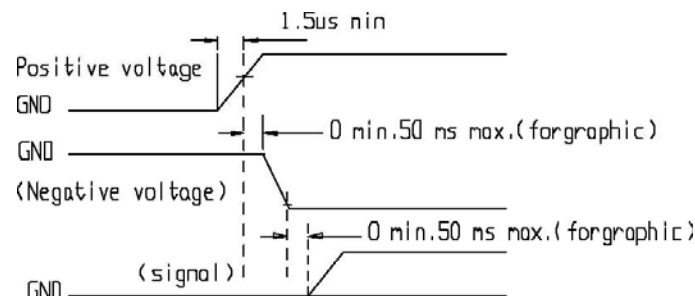
(3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.

(4) If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.

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(5) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit. Therefore, it must be used under the relative condition of 40 °C , 50% RH.

(6) When turning the power on, input each signal after the positive/negative voltage becomes stable.



### Storage

When storing LCDs as spares for some years, the following precaution are necessary.

- (1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for dessicant.
- (2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0 °C and 35 °C.
- (3) The polarizer surface should not come in contact with any other objects. (We advise you to store them in the container in which they were shipped.)

### Safety

- (1) It is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
- (2) If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

### Return LCM under warranty

No warranty can be granted if the precautions stated above have been disregarded.

The typical examples of violations are :

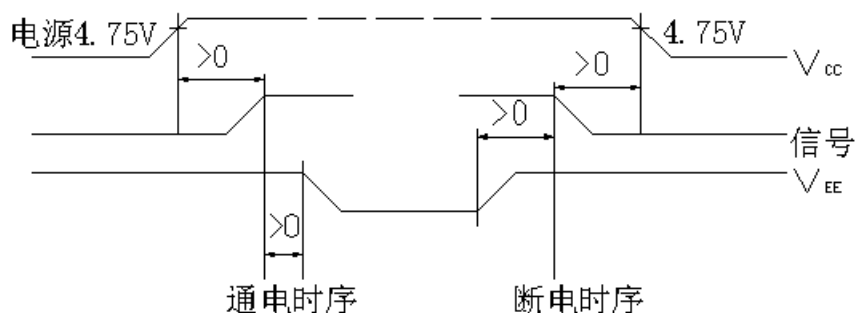
- Broken LCD glass.
- PCB eyelet's damaged or modified.
- PCB conductors damaged.
- Circuit modified in any way, including addition of components.

- 
- PCB tampered with by grinding, engraving or painting varnish.
  - soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelet's, conductors and terminals.

## 液晶显示模块使用注意事项

1. 请勿随意自行加工、整修、拆卸。
2. 避免对液晶屏表面施加压力。
3. 不要用手随意去摸外引线、电路板上的电路及金属框。
4. 如必须直接接触时，应使人体与模块保持同一电位，或将人体良好接地。
5. 焊接使用的烙铁、操作用的电动改锥等工具必须良好接地，没漏电。
6. 严防各种静电。
7. 模块使用接入电源及断开电源时，必须按图时序进行。即必须在正电源（ $5 \pm 0.25V$ ）稳定接入后，才能输入信号电平。如在电源稳定接入前，或断开后就输入信号电平，将会损坏模块中的集成电路，使模块损坏。



8. 点阵模块在调节时，应调整 VEE 至最佳对比度、视角时为止。如果 VEE 调整过高，不仅会影响显示，还会缩短液晶的寿命。
9. 模块表面结雾时，不要通电工作，因为这将引起电极化学反应，产生断线。
10. 模块要存储在暗处（避阳光），温度在 $-10^{\circ}\text{C} \sim +35^{\circ}\text{C}$ ，湿度在 RH60%以上的地方。如能装入聚乙烯口袋（最好有防静电涂层）并将口封住最好。

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服务电话：010-52926620, 82626833

公司地址：北京市中关村大街 32 号蓝天和盛大厦 811 室